Concept Notes on Semicondoctor Electronics:Materials,Devices and Simple Circuits for NEET

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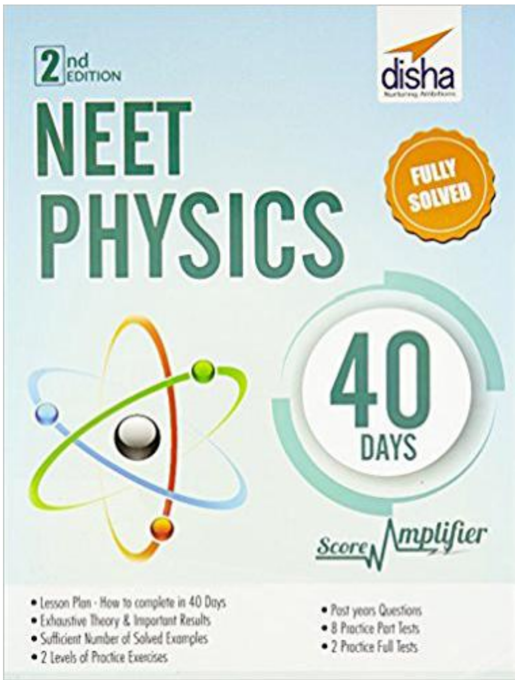

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Product Description : NEET Physics 40 Days Score Amplifier 2nd Edition is developed for quick revision and practice of the complete syllabus of the NEET exams in a short span of 40 days. The book can prove to the ideal material for class 12 students as they can utilise this book to revise their preparation immediately after the board exams.

• The book follows the Syllabus and chapter plan as per the NCERT books of class 11 and 12.

• The book contains 30 chapters divided into 8 units. Each unit provides a Practice Test along with detailed solutions. At the end 2 Mock Tests based on the full syllabus are provided.

• Each chapter provides exhaustive theory explaining all fundamentals/concepts to build a strong base.

• This is followed by a set of 2 exercises for practice. The first exercise is a basic exercise whereas the second exercise is advanced.

• The solutions to the exercises have been provided immediately at the end of each chapter.

• The book covers past questions of the various entrance exams which have been incorporated in the exercises of the respective chapters.

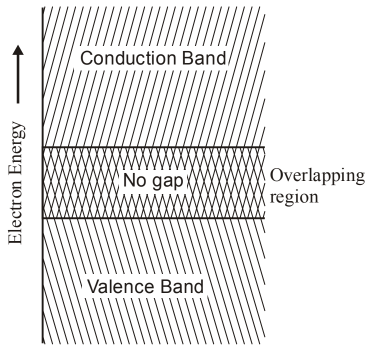
Chapter

29 SEMICONDUCTOR ELECTRONICS : MATERIALS, DEVICES AND SIMPLE CIRCUITS

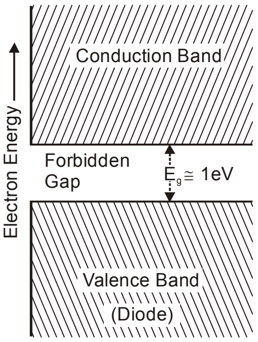
Concepts

ENERGY BANDS IN SOLIDS

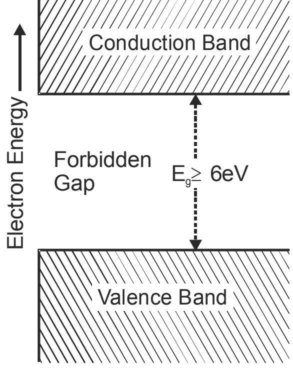
There are two distinct band of energies **valence band** and **conduction band** in which the electrons in a material lie. Valence band energies are low as compared to conduction band energies. All energy levels in the valence band are filled while energy levels in the conduction band may be fully empty or partially filled. The electrons in the conduction band are free to move in a solid and are responsible for the conductivity. The extent of conductivity depends upon the energy gap (E_g) between the top of valence band (E_V) and the bottom of the conduction band E_C. The electrons from valence band can be excited by heat, light or electrical energy to the conduction band and thus, produce a change in the current flowing in a semiconductor.



Conductor



Semiconductor



Insulator

SEMICONDUCTOR ELECTRONICS

Semiconductors are the basic materials used in the present solid state electronic devices like diode, transistor, ICs, etc.

Lattice structure and the atomic structure of constituent elements decide whether a particular material will be insulator, conductor or semiconductor.

Conductors have low resistivity (10^{-2} to 10^{-8} Ωm), **insulators** have very high resistivity ($>10^8$ Ωm^{-1}), while **semiconductors** have intermediate values of resistivity.

Semiconductors are elemental (Si, Ge) as well as compound (GaAs, CdS etc.).

Pure semiconductors are called **'intrinsic semiconductors'.** The presence of charge carriers (electrons and holes) is an 'intrinsic' property of the material and these are obtained as a result of thermal excitation. The number of electrons (n_e) is equal to the number of holes (n_h) in intrinsic semiconductors. Holes are essentially electron vacancies with an effective positive charge.

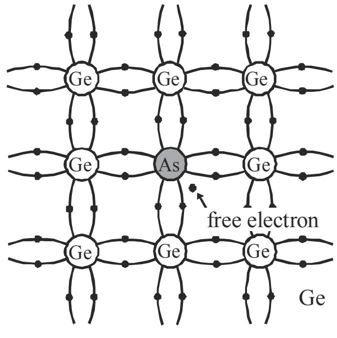
The number of charge carriers can be changed by 'doping' of a suitable impurity in pure semiconductors. Such semiconductors are known as **extrinsic semiconductors.**

Types of Extrinsic Semiconductors

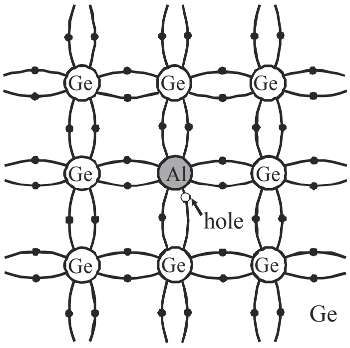
There are two types of extrinsic semiconductors (n-type and p-type).

(i) In n-type Semiconductors, $n_e >> n_h$

n-type semiconducting Si or Ge is obtained by doping with pentavalent atoms (donors) like As, Sb, P, etc.,



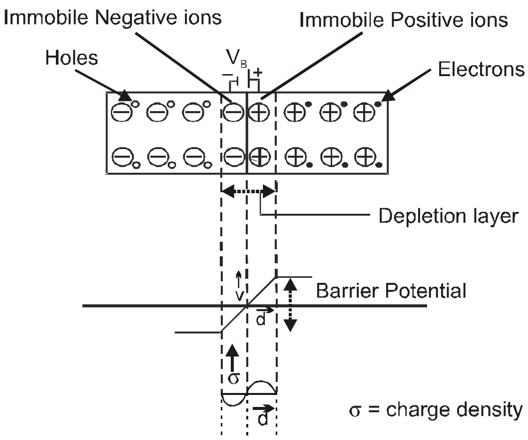
(ii) In p-type semiconductors, $n_h >> n_e$
p-type Si or Ge can be obtained by doping with trivalent atom (acceptors) like B, Al, In etc.



$n_e n_h = n_i^2$ in all cases. Further, the material possesses an overall charge neutrality.

p-n JUNCTION

p-n junction is the 'key' to all semiconductor devices. When such a junction is made, a 'depletion layer' is formed consisting of immobile ion-cores devoid of their electrons or holes. This is responsible for a junction potential barrier.

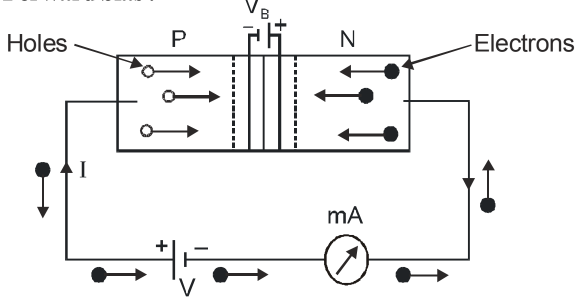


The p-n junction can be assumed as a capacitor having the depletion layer acting as a capacitor.

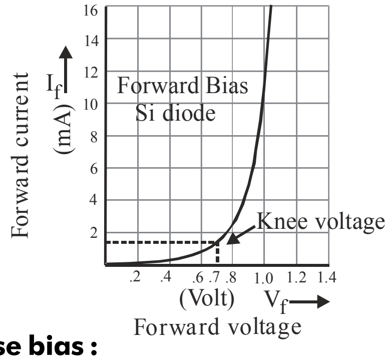
FORWARD AND REVERSE BIAS

By changing the external applied voltage, junction barriers can be changed. In forward bias (n-side is connected to negative terminal of the battery and p-side is connected to the positive), the barrier is decreased while the barrier increases in reverse bias. Hence, forward bias current is more (mA) while it is very small (μA) in a p-n junction diode.

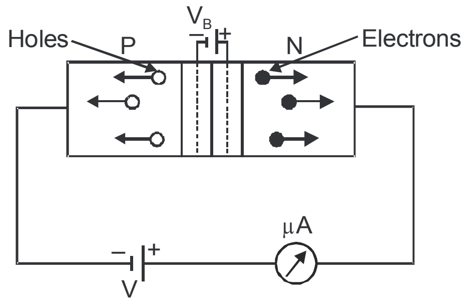
Forward bias :



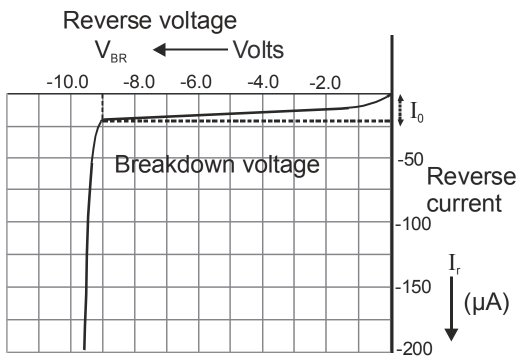
I-V Characteristics in Forward Bias



Reverse bias :

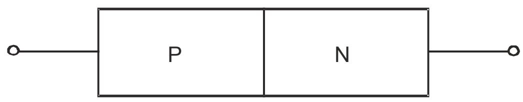


I-V Characteristics in Reverse Bias

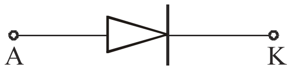


DIODE AS A RECTIFIER

Diodes can be used for rectifying an ac voltage (restricting the ac voltage to one direction).

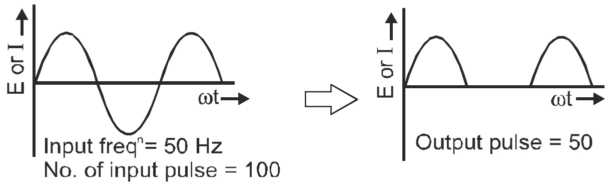


Symbol of Diode

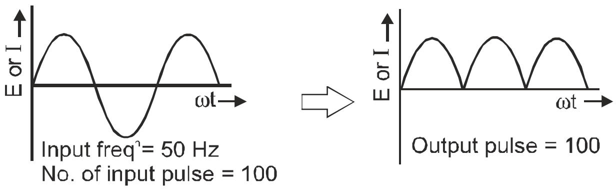


With the help of a capacitor or a suitable filter, a dc voltage can be obtained.

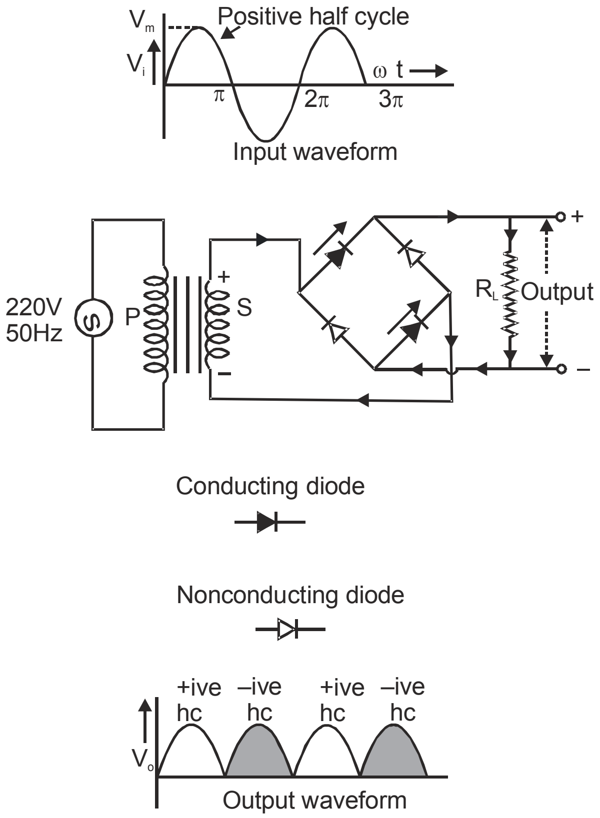
Half wave rectifier



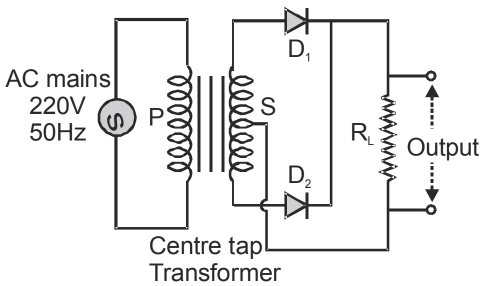
Full wave rectifier

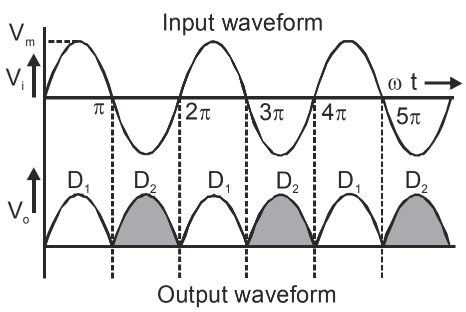


Bridge circuit as a full wave rectifier.



Central tapping circuit as a full wave amplifier.



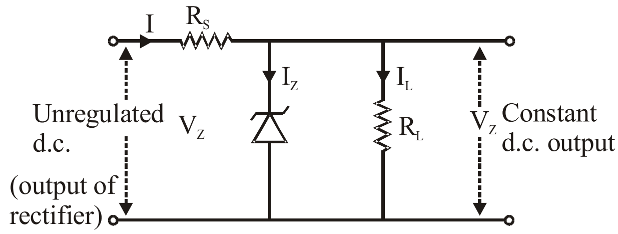


SOME SPECIAL DIODES

There are some special purpose diodes.

Zener diode is one such special purpose diode. In reverse bias, after a certain voltage, the current suddenly increases (breakdown voltage) in a Zener diode. This property has been used to obtain **voltage regulation**.

Zener diode



p-n junctions have also been used to obtain many photonic or optoelectronic devices where one of the participating entity is 'photon':

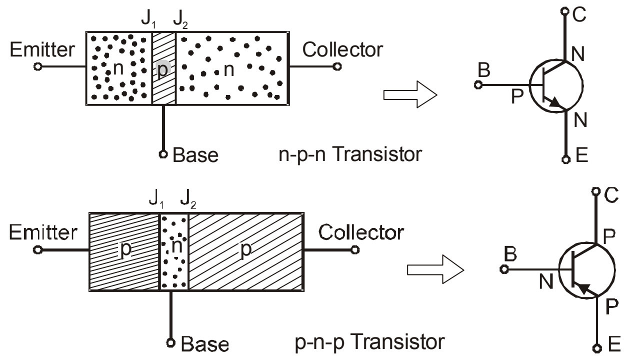
(a) **Photodiodes** in which photon excitation results in a change of reverse saturation current which helps us to measure light intensity;

(b) **Solar cells** which convert solar energy into electricity;

(c) **Light Emitting Diode (LED) and Diode Laser** in which electron excitation by a bias voltage results in the generation of light.

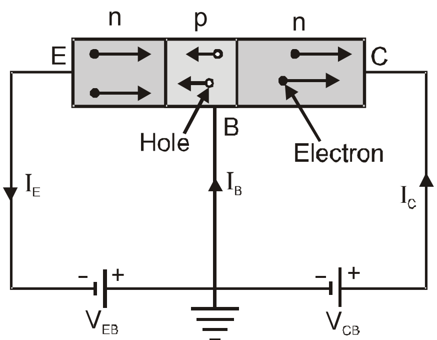
JUNCTION TRANSISTOR

Transistor is an n-p-n or p-n-p junction device.



The central block (thin and lightly doped) is called 'Base' while the other electrodes are 'Emitter' and 'Collector'. The emitter-base junction is forward biased while collector-base junction is reverse biased.

In transistors, the base region is both narrow and lightly doped, otherwise the electrons or holes coming from the input side (say, emitter in CE-configuration) will not be able to reach the collector



Working of transistor : Fig. shows a common base configuration of p-n-p transistor. The forward biasing of emitter junction lowers the emitter base potential barrier height, whereas the reverse biasing of collector junction increases the collector-base potential barrier height. Hence holes (majority carriers in p-type) flows through emitter to base and constitutes an emitter current I_E. Since emitter is heavily doped in comparison to base, so approximately (only 5% holes recombine with electrons in base region and constitute base current I_B) 95% holes reach to collector and constitute collector current I_C. From Kirchoff's current Law,

$$I_E = I_C + I_B \qquad ...(1)$$

Eq. (1) holds true regardless of circuit configuration or transistor type (p-n-p or n-p-n) that is used.

The **current gain** of transistor is defined as ratio of collector current I_C to base current I_B i.e.,

$$\beta = \frac{I_c}{I_B} \qquad ...(2)$$

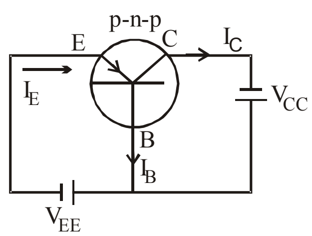


Fig.

The value of β lies between 10 and 100.

Since $I_E \approx I_C$ and exactly

$$I_E = \alpha I_C \qquad ...(3)$$

Whereas α is defined as the ratio of collector current I_C to emitter current I_E. The value of α is always less than unity. In terms of β, α is

$$\alpha = \frac{\beta}{1+\beta} \Rightarrow \beta = \frac{\alpha}{1-\alpha} \qquad ...(4)$$

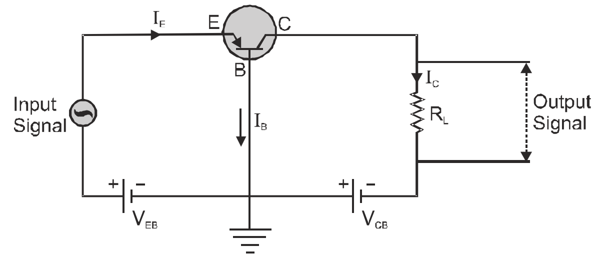
The transistors can be connected in such a manner that either C or E or B is common to both the input and output. This gives the three configurations in which a transistor is used: Common Emitter (CE), Common Collector (CC) and Common Base (CB). The plot between I_C and V_{CE} for fixed I_B is called **output characteristics** while the plot between I_B and V_{BE} with fixed V_{CE} is called **input characteristics**. The important transistor parameters for CE-configuration are:

Input resistance, $r_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE}}$

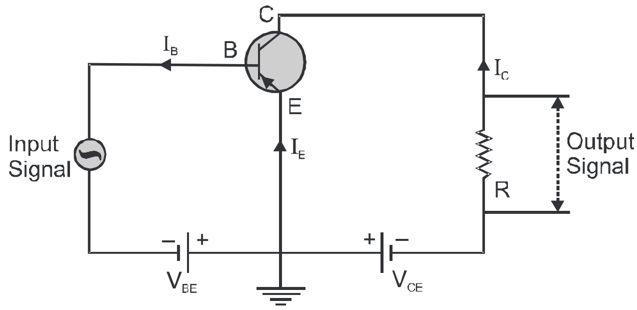
Output resistance, $r_0 = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B}$

Current amplification factor, $\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}}$

(i) **Common Base (C.B.) configuration**



(ii) **Common Emitter (C.E.) configuration**



(iii) **Common Collector (C.C) configuration :** Here the collector terminal is common to both input as well as output terminals as shown in fig. The base terminal is input & Emitter is output terminal.

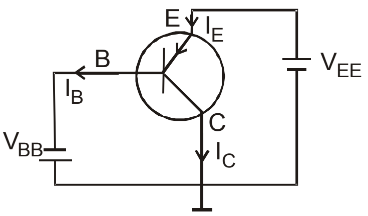


Fig.

TRANSISTOR AS AN AMPLIFIER, AN OSCILLATOR AND A SWITCH

Transistor can be used as an **amplifier** and **oscillator**. In fact, an oscillator can also be considered as a self-sustained amplifier in which a part of output is feed-back to the input in the same phase (positive feed back). The voltage gain of a transistor amplifier in common emitter configuration is:

$A_v = \left(\frac{V_0}{V_i}\right) = \beta\frac{R_C}{R_B}$, where R_C and R_B are respectively the resistances in collector and base sides of the circuit.

In an **oscillator**, the feedback is in the same phase (positive feedback). If the feedback voltage is in opposite phase (negative feedback), the gain is less than 1 and it can never work as oscillator. It will be an amplifier with reduced gain. However, the negative feedback also reduces noise and distortion in an amplifier which is an advantageous feature.

The frequency of oscillator $f = \frac{1}{2\pi\sqrt{LC}}$

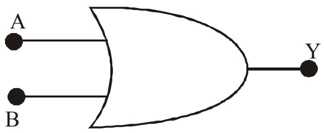
When the transistor is used in the cutoff or saturation state, it acts as a **switch**.

LOGIC GATES

There are some special circuits which handle the digital data consisting of 0 and 1 levels. This forms the subject of **Digital Electronics.**

The important digital circuits performing special logic operations are called **logic gates**. These are: OR, AND, NOT, NAND, and NOR gates.

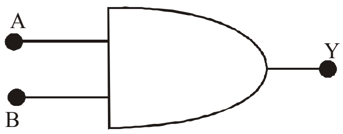
(a) OR gate :



Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Boolean expression : $A + B = Y$

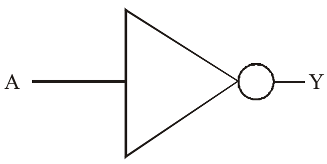
(b) AND gate :



Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Boolean expression : $A . B = Y$

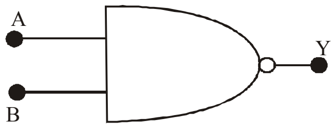
(c) NOT gate : **Truth table**



Input	Output
A	Y
0	1
1	0

Boolean expression : $\overline{A} = Y$

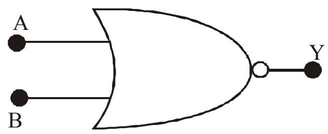
(d) NAND gate :



Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Boolean expression : $\overline{A \cdot B} = Y$

(e) NOR gate :



Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

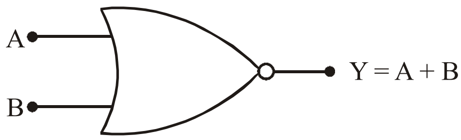
Boolean expression : $\overline{A + B} = Y$

The NOR gate : The output is high, when all inputs are low.

Truth Table:

A	**B**	**Y**
0	0	1
1	0	0
0	1	0
1	1	0

Logic Symbols



Boolean expression : $\overline{A + B} = Y$

In modern day circuit, many logical gates or circuits are integrated in one single 'Chip'. These are known as **Integrated circuits (IC)**.

Important Results

1. In a transistor circuit the reverse bias is high as composed to the forward bias. So that it may exert a large attractive force on the charge carriers to enter the collector region.
2. Semiconductor devices are current control devices.
3. The electric field setup across the potential barrier is of the order of 3×10^5 V/m for Ge and 7×10^5 V/m for Si.
4. Voltage obtained from a diode rectifier is a mixture of alternating and direct voltage.
5. Number of conduction electrons per unit volume

$$= \frac{\text{Material's density}}{(\text{Molar mass M})/N_A}$$

N_A = Avogadro's number = 6.023×10^{23}/mol

6. Current flowing through a semiconductor is given by

$$I = I_e + I_h = e_A (N_e \mu_e + N_h \mu_h)$$

7. Conductivity of the semiconductor is given by

$$\sigma = e(n_e \mu_e + n_h \mu_h)$$

8. For transistor, $I_e = I_b + I_c$
9. α and β are related as

$$\beta = \frac{\alpha}{1-\alpha}$$

$$\beta_{a.c.} = \left(\frac{\Delta I_c}{\Delta I_b}\right) V_{ce} = \text{constant}$$

10. Transconductances

$$g_m = \frac{\Delta I_C}{\Delta V_{BE}} = \frac{\beta}{R_{in}}$$

Miscellaneous Solved Examples

Example 1 :

Can we take one slab of p-type semiconductor and physically join it to another n-type semiconductor to get p-n junction?

Sol. No! Any slab, howsoever flat, will have roughness much larger than the inter-atomic crystal spacing (~2 to 3 Å) and hence continuous contact at the atomic level will not be possible. The junction will behave as a discontinuity for the flowing charge carriers.

Example 2 :

C, Si and Ge have same lattice structure. Why is C insulator while Si and Ge intrinsic semiconductors ?

Sol. The 4 bonding electrons of C, Si or Ge lie, respectively, in the second, third and fourth orbit. Hence, energy required to take out an electron from these atoms (i.e., ionisation energy E_g) will be least for Ge, followed by Si and highest for C. Hence, number of free electrons for conduction in Ge and Si are significant but negligibly small for C.

Example 3 :

In a Zener regulated power supply a Zener diode with V_Z = 6.0 V is used for regulation. The load current is to be 4.0mA and the unregulated input is 10.0 V. What should be the value of series resistor R_S ?

Sol. The value of R_S should be such that the current through the Zener diode is much larger than the load current. This is to have good load regulation. Choose Zener current as five times the load current, i.e., I_Z = 20 mA. The total current through R_S is, therefore, 24 mA. The voltage drop across R_S is 10.0 – 6.0 = 4.0 V. This gives $R_S = 4.0V/(24 \times 10^{-3})A = 167\ \Omega$. The nearest value of carbon resistor is 150 Ω. So, a series resistor of 150 Ω is appropriate. Note that slight variation in the value of the resistor does not matter, what is important is that the current I_Z should be sufficiently larger than I_L.

Example 4 :

In a p-n-p transistor circuit, the collector current is 10mA. If 90% of the hole reach the collector, find emitter and base currents.

Sol. Collector current I_c = 10 mA

Now, I_c = 90% of I_e

$$I_c = \frac{90}{100} I_e = 0.9\ I_e$$

$$I_e = \frac{I_c}{0.9} = \frac{10mA}{0.9} = 11.1mA$$

Now, $I_e = I_b + I_c$

$11.1\ mA = I_b + 10mA$

$I_b = 1.1\ mA$

Example 5 :

The current in the forward bias is known to be more (~mA) than the current in the reverse bias (~μA). What is the reason then to operate the photodiodes in reverse bias ?

Sol. Consider the case of an n-type semiconductor. Obviously, the majority carrier density (n) is considerably larger than the minority hole density p (i.e., n >> p). On illumination, let the excess electrons and holes generated be Δn and Δp, respectively:

$n' = n + \Delta n$

$p' = p + \Delta p$

Here n' and p' are the electron and hole concentrations at any particular illumination and n and p are carriers concentration when there is no illumination.

Remember Δn = Δp and n >> p.

Example 6 :

A full wave rectifier uses two diodes, the internal resistance of each diode is 20Ω. The transformer r.m.s. secondary voltage from centre tap to each end of secondary is 50V and load resistance is 980Ω. Find

(i) The mean load current

(ii) The r.m.s. value of load current

Sol. Input resistance R_i = 20Ω

Output resistance R_L = 980 Ω

r.m.s. value of voltage = 50V [V_0 is maximum voltage]

$$V_{rms} = \frac{V_0}{\sqrt{2}} \quad \text{or} \quad V_0 = \sqrt{2}V_{rms} = \sqrt{2} \times 50 = 70.7V$$

Total resistance = $R_i + R_C$ = 20 + 980 = 1000 Ω

So, the maximum load current

$$I_0 = \frac{V_0}{\text{Total resistance}}$$

$$I_0 = \frac{70.7}{1000} = 70.7 \times 10^{-3} = 70.7mA$$

(i) Now, the mean load current

$$I_{d.c.} = \frac{2}{\pi} I_0 = \frac{2}{3.14} \times 70.7 \times 10^{-3} = 45\ mA$$

(ii) R.M.S. value of load current

$$I_{rms} = \frac{I_0}{\sqrt{2}} = \frac{70.7 \times 10^{-3}}{1.41} = 50\ mA$$

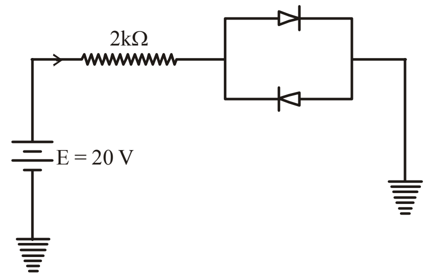
Exercise 1

1. p-n junction diode works as a insulator, if connected
   (a) to A.C. (b) in forward bias
   (c) in reverse bias (d) None of these
2. A transitor is connected is common emitter configuration. The collector supply is 8 V and the voltage drop across a resistor of 800Ω in the collector circuit is 0.5 V. If the current gain factor (α) is 0.96, then base current will be
   (a) 24 μA (b) 26 μA
   (c) 28 μA (d) 30 μA
3. In an n-type silicon, which of the following statement is true?
   (a) Electrons are majority carriers and trivalent atoms are the dopants.
   (b) Electrons are minority carriers and pentavalent atoms are the dopants.
   (c) Holes are minority carriers and pentavalent atoms are the dopants.
   (d) Holes are majority carriers and trivalent atoms are the dopants.
4. Which of the statements is true for p-type semiconductos?
   (a) Electrons are majority carriers and trivalent atoms are the dopants.
   (b) Electrons are minority carriers and pentavalent atoms are the dopants.
   (c) Holes are minority carriers and pentavalent atoms are the dopants.
   (d) Holes are majority carriers and trivalent atoms are the dopants.
5. Carbon, silicon and germanium have four valence electrons each. These are characterised by valence and conduction bands separated by energy band gap respectively equal to $(E_g)_C$, $(E_g)_{Si}$ and $(E_g)_{Ge}$. Which of the following statements is true?
   (a) $(E_g)Si < (E_g)Ge < (E_g)C$ (b) $(E_g)C < (E_g)Ge > (E_g)Si$
   (c) $(E_g)C > (E_g)Si > (E_g)Ge$ (d) $(E_g)C = (E_g)Si = (E_g)Ge$
6. In a junction diode, the holes are due to
   (a) protons (b) neutrons
   (c) extra electrons (d) missing of electrons
7. In an unbiased p-n junction, holes diffuse from the p-region to n-region because
   (a) free electrons in the n-region attract them
   (b) they move across the junction by the potential difference
   (c) hole concentration in p-region is more as compared to n-region
   (d) All the above
8. When a forward bias is applied to a p-n junction, it
   (a) raises the potential barrier.
   (b) reduces the majority carrier current to zero.
   (c) lowers the potential barrier.
   (d) None of these.
9. The potential barrier, in the depletion layer, is due to
   (a) ions (b) holes
   (c) electrons (d) both (b) and (c)
10. Avalanche breakdown is due to
    (a) collision of minority charge carrier
    (b) increase in depletion layer thickness
    (c) decrease in depletion layer thickness
    (d) None of these
11. In a semiconductor
    (a) there are no free electrons at any temperature
    (b) the numbe of free electrons is more than that in a conductor
    (c) there are no free electrons at 0K
    (d) None of these
12. Zener diode is used as
    (a) half wave rectifier (b) full wave rectifier
    (c) ac voltage stabilizer (d) dc voltage stabilizer
13. For a transistor amplifier, the voltage gain
    (a) remains constant for all frequencies
    (b) is high at high and low frequencies and constant in the middle frequency range
    (c) is low at high and low frequencies and constant at mid frequencies
    (d) None of these
14. The value of β for a transistor, for which α = 0.95, will be
    (a) 19 (b) 91
    (c) 1.9 (d) 0.19
15. In a semiconductor, the concentration of electrons is $8 \times 10^{14}/cm^3$ and that of the holes is 5×10^{12} cm^3. The semiconductor is
    (a) p-type (b) n-type
    (c) intrinsic (d) pnp-type
16. When a semiconductor is heated, its resistance
    (a) decreases (b) increases
    (c) remains unchanged (d) nothing is definite
17. The forbidden gap in the energy bands of germanium at room temperature is about
    (a) 1.1 eV (b) 0.1 eV
    (c) 0.67 eV (d) 6.7 eV
18. To obtain a p-type germanium semiconductor, it must be doped with
    (a) Arsenic (b) Antimony
    (c) Indium (d) Phosphorus
19. Which impurity is doped in Si to form n-type semi-conductors?
    (a) Al (b) B
    (c) As (d) None of these
20. In a p-type semi-conductor, germanium is dopped with
    (a) Gallium (b) Boron
    (c) Aluminium (d) All of these
21. In extrinsic semiconductors
    (a) the conduction band and valence band overlap
    (b) the gap between conduction band and valence band is more than 16 eV
    (c) the gap between conduction band and valence band is near about 1 eV
    (d) the gap between conduction band and valence band will be 100 eV and more

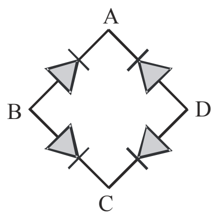
22. Function of rectifier is
(a) to convert ac into dc (b) to convert dc into ac
(c) Both (a) and (b) (d) None of these
23. Zener breakdown takes place if
(a) doped impurity is low (b) doped impurity is high
(c) less impurity in n-part (d) less impurity in p-part
24. Which one of the following is NOT a correct statement about semiconductors?
(a) The electrons and holes have different mobilities in a semiconductor
(b) In an n-type semiconductor, the Fermi level lies closer to the conduction band edge
(c) Silicon is a direct band gap semiconductor
(d) Silicon is has diamond structure
25. The donor level in a semiconductor is placed:
(a) half-way in the forbidden energy gap
(b) in the forbidden energy gap close to the upper edge of the valence band
(c) in the conduction band close to the lower edge to the conduction band
(d) in the forbidden energy gap close to the lower edge of the conduction band
26. The energy band gap is maximum in
(a) metals (b) superconductors
(c) insulators (d) semiconductors.
27. An oscillator is nothing but an amplifer with
(a) positive feedback (b) negative feedback
(c) large gain (d) no feedback

Exercise 2

1. Holes are charge carriers in
1 Intrinsic semiconductors 2. Ionic solids
3. p-type semiconductors 4. Metals
Correct options are
(a) 1 and 3 (b) 1 and 4
(c) 1 and 2 (d) 1, 2 and 3
2. Assuming the diodes to be of silicon with forward resistance zero, the current I in the following circuit is



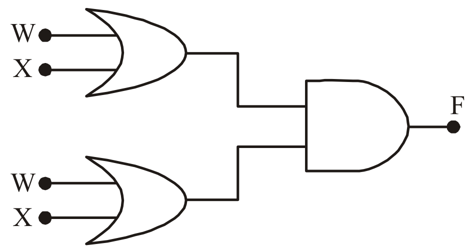
(a) 0 (b) 9.65 mA
(c) 10 mA (d) 10.35 mA
3. When a solid with a band gap has a donor level just below its empty energy band, the solid is
(a) an insulator (b) a conductor
(c) *p*-type semiconductor (d) *n*-type semiconductor
4. To obtain P-type Si semiconductor, we need to dope pure Si with
(a) Aluminium (b) Phosphorous
(c) Oxygen (d) Germanium.
5. For transistor action, which of the following statements are correct
(1) Base, emitter and collector regions should have similar size and doping concentrations
(2) The base region must be very thin and lightly doped
(3) The emitter junction is forward biased and collector junction is reverse biased
(4) Both the emitter junction as well as the collector junction are forward biased
Correct options are
(a) 2 and 3 (b) 1 and 2
(c) 1 and 3 (d) 1, 3 and 4
6. In the diagram, the input is across the terminals A and C and the output is across the terminals B and D, then the output is



(a) zero
(b) same as input
(c) full wave rectifier
(d) half wave rectifier
7. In a full wave rectifiers, input ac current has a frequency 'ν'. The output frequency of current is
(a) ν/2 (b) ν
(c) 2ν (d) None of these
8. Which of the following statements is not true?
(a) The potential is the same everywhere
(b) The p-type is a higher potential than the n-type side
(c) There is an electric field at the junctiuon directed from the n-type side to the p-type side
(d) There is an electric field at the junction directed from the p-type side to the n-type side
9. In the circuit given below, the value of the current is

(a) 0 (b) 10^{-2} A
(c) 10^{2} A (d) 10^{-3} A
10. Regarding a semiconductor which one of the following is wrong?
(a) There are no free electrons at room temperature
(b) There are no free electrons at 0K
(c) The number of free electrons increases with rise of temperature
(d) The charge carriers are electrons and holes
11. For a CE transistor amplifier, the audio signal voltage across the collector resistance of 2.0 kΩ is 2.0 V. Suppose the current amplification factor of the transistor is 100, What should be the value of R_B in series with V_{BB} supply of 2.0V if the dc base current has to be 10 times the signal current?
(a) 14 kΩ (b) 18 kΩ
(c) 10 kΩ (d) 5 kΩ
12. In the above question, calculate the dc drop across the collector resistance.
(a) 20 mA (b) 10 mA
(c) 30 mA (d) 50 mA

13. The diagram of a logic circuit is given below.

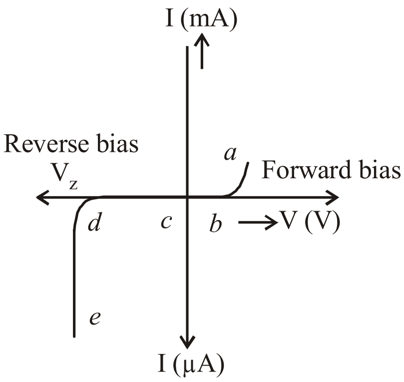


The output F of the circuit is given by

(a) W. (X + Y) (b) W. (X. Y)

(c) W + (X. Y) (d) W + (X + Y)

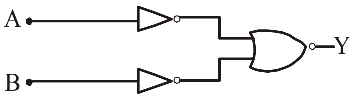
14. The graph given below represents the I-V characteristic of a Zener diode. Which part of the characteristic curve is most relevant for its operation as a voltage regulator ?

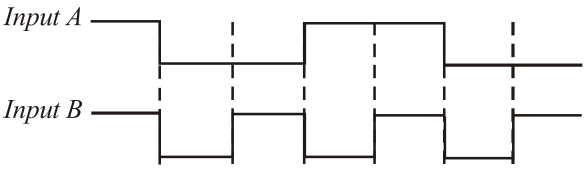


(a) *a b* (b) *b c*

(c) *c d* (d) *d e*

15. The logic circuit shown below has the input waveforms '*A*' and '*B*' as shown. Pick out the correct output waveform.

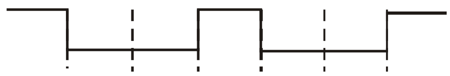


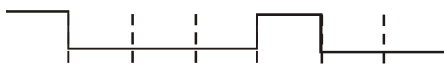


Output is

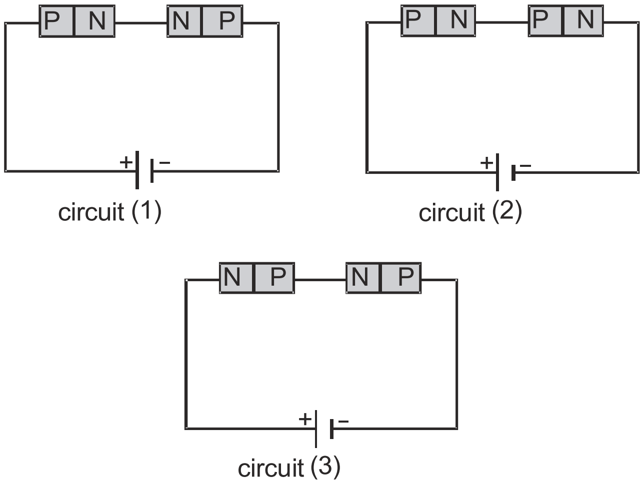
(a) 

(b) 

(c) 

(d) 

16. Two indentical P-N junction may be connected in series with a battery in three ways (figure). The potential drops across the two P-N junction are equal in



(a) Circuit 1 and 2 (b) Circuit 2 and 3

(c) Circuit 3 and 1 (d) Circuit 1 only

17. An n-type silicon sample of of width 4×10^{-3} m, thickness 25×10^{-5} m and length 6×10^{-2} m carries a current of 4.8mA when the voltage is applied across the length of the sample. What is the current density ? If the free electron density is $10^{22}/m^3$ then find how much time does it take for the electron to travel the full length of the sample ?

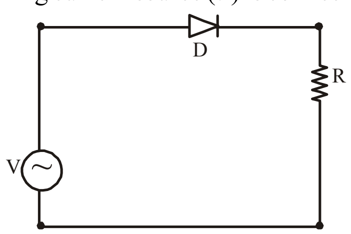
(a) 4.8×10^3 A/m^2, 2×10^{-2} sec.

(b) 1.8×10^3 A/m^2, 2×10^{-2} sec.

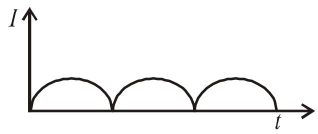
(c) 3.3×10^3 A/m^2, 2.2×10^{-2} sec.

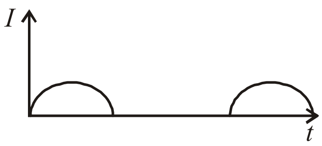
(d) 5.2×10^3 A/m^2, 4×10^{-2} sec.

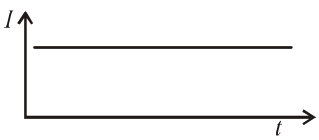
18. A *p-n* junction (*D*) shown in the figure can act as a rectifier. An alternating current source (*V*) is connected in the circuit.

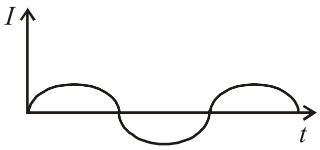


The current (*I*) in the resistor (*R*) can be shown by :

(a) 

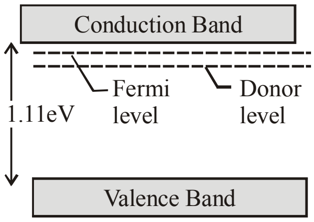
(b) 

(c) 

(d) 

DIRECTIONS for Qs. 19 and 20 : Read the passage given below and answer the questions that follow :

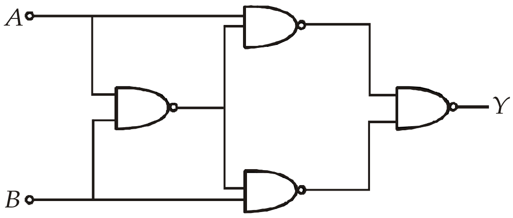
Doping changes the fermi energy of a semiconductor. Consider silicon, with a gap of 1.11 eV between the top of the valence bond and the bottom of the conduction band. At 300K the Fermi level of the pure material is nearly at the midpoint of the gap. Suppose that silicon is doped with donor atoms, each of which has a state 0.15 eV below the bottom of the silicon conduction band, and suppose further that doping raises the Fermi level to 0.11 eV below the bottom of that band.



19. For both pure and doped silicon, calculate the probability that a state at the bottom of the silicon conduction band is occupied?
(a) 5.20×10^{-2} (b) 1.40×10^{-2}
(c) 10.5×10^{-2} (d) 14×10^{-2}

20. Calculate the probability that a donor state in the doped material is occupied?
(a) 0.824 (b) 0.08
(c) 0.008 (d) 8.2

21. Truth table for system of four NAND gates as shown in figure is :



(a)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

(b)

A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

(c)

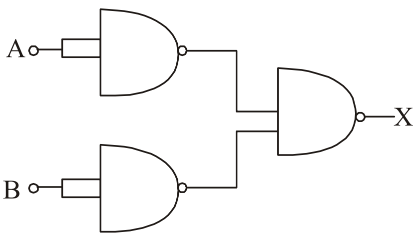
A	B	Y
0	0	1
0	1	1
1	0	0
1	1	0

(d)

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	1

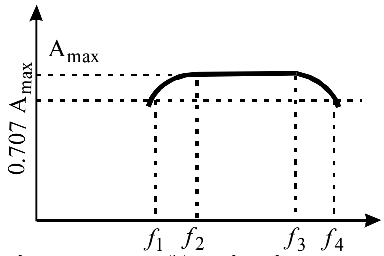
22. The output of an OR gate is connected to both the inputs of a NAND gate. The combination will serve as a:
(a) NOT gate (b) NOR gate
(c) AND gate (d) OR gate

23. The combination of gates shown below yields



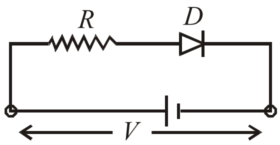
(a) OR gate (b) NOT gate
(c) XOR gate (d) NAND gate

24. The frequency response curve of RC coupled amplifier is shown in figure. The band with of the amplifier will be



(a) $f_3 - f_2$ (b) $f_4 - f_1$
(c) $\frac{f_4 - f_2}{2}$ (d) $f_3 - f_1$

25. A d.c. battery of V volt is connected to a series combination of a resistor R and an ideal diode D as shown in the figure below. The potential difference across R will be



(a) $2V$ when diode is forward biased
(b) Zero when diode is forward biased
(c) V when diode is reverse biased
(d) V when diode is forward biased

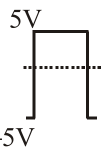
26. The following truth table belongs to which of the following four gates?

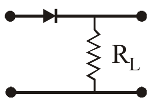
A	B	Y
1	1	0
1	0	0
0	1	0
0	0	1

(a) NOR (b) XOR
(c) NAND (d) OR

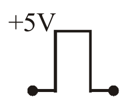
27. An n-p-n transistor conducts when
(a) both collector and emitter are negative with respect to the base
(b) both collector and emitter are positive with respect to the base
(c) collector is positive and emitter is negative with respect to the base
(d) collector is positive and emitter is at same potential as the base

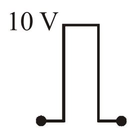
28. If in a p-n junction diode, a square input signal of 10 V is applied as shown

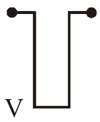


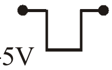


Then the output signal across R_L will be

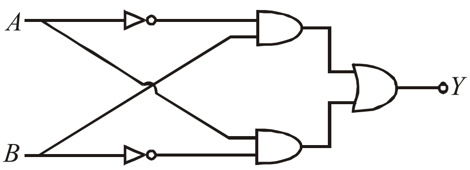
(a) 

(b) 

(c) 

(d) 

29. The following circut represents



(a) OR gate (b) XOR gate
(c) AND gate (d) NAND gate

30. A piece of copper and other of germanium are cooled from the room temperature to 80 K, then
(a) resistance of each will increase
(b) resistance of copper will decrease
(c) resistance of copper will increase while that of germanium will decrease
(d) resistance of copper will decrease while that of germanium will increase

DIRECTIONS for Qs. 31 to 33 : These are Assertion-Reason type questions. Each of these questions contains two statements: Statement-1 (Assertion) and Statement-2 (Reason). Answer these questions from the following four options.
(a) Statement -1 is false, Statement-2 is true
(b) Statement -1 is true, Statement-2 is true; Statement -2 is a correct explanation for Statement-1
(c) Statement -1 is true, Statement-2 is true; Statement -2 is not a correct explanation for Statement-1
(d) Statement -1 is true, Statement-2 is false

31. Statement-1 : When two semi conductor of *p* and *n* type are brought in contact, they form *p-n* junction which act like a rectifier.
Statement-2 : A rectifier is used to convert alternating current into direct current.

32. Statement-1 : NAND or NOR gates are called digital building blocks.
Statement-2 : The repeated use of NAND (or NOR) gates can produce all the basis or complicated gates.

33. Statement-1 : NOT gate is also called invertor circuit.
Statement-2 : NOT gate inverts the input order.

Hints & Solutions

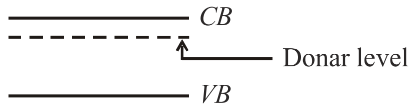
EXERCISE - 1

1. **(c)** In reverse bias no current flows.

2. **(b)** Current gain $\beta = \frac{I_c}{I_b} = \frac{\alpha}{1-\alpha} = \frac{0.96}{1-0.96} = 24$

$\therefore I_b = \frac{I_c}{24} = \frac{0.5}{800 \times 24} = 26\,\mu A$

3. **(c)** 4. **(d)** 5. **(c)** 6. **(d)** 7. **(c)**
8. **(c)** 9. **(a)**
10. **(a)** At high reverse voltage, the minority charge carriers, acquires very high velocities. These by collision break down the covalent bonds, generating more carriers. This mechanism is called Avalanche breakdown.
11. **(c)** At 0K semiconductor behaves as an insulator.
12. **(c)** For a wide range of values of load resistance, the current in the zener diode may change but the voltage across it remains unaffected. Thus the output voltage across the zener diode is a regulated voltage.
13. **(c)**
14. **(a)** $\beta = \frac{\alpha}{1-\alpha} = \frac{0.95}{1-0.95} = \frac{0.95}{0.05} = 19$
15. **(b)** Since $n_e > n_h$, the semiconductor is N-type
16. **(a)**
17. **(c)** $\Delta E_{g(Germanium)} = 0.67$ eV
18. **(c)** For p-type semiconductor the doping impurity should be trivalent.
19. **(c)** Because As is pentavalent impurity.
20. **(d)** Gallium, boron and aluminium are trivalent.
21. **(c)**
22. **(a)** ac → Rectifier → dc
23. **(b)** Zener breakdown can occur in heavily doped diodes. In lightly doped diodes the necessary voltage is higher, and avalanche multiplication is then the chief process involved.
24. **(c)** Silicon is an indirect-band gap semi- conductor.



25. **(d)**
26. **(c)** Maximum in insulators and overlaping in metals
27. **(a)** A positive feedback from output to input in an amplifier provides oscillations of constant amplitude.

EXERCISE - 2

1. **(a)** In Intrinsic semiconductors, electrons and holes both are charge carriers. In p-type semiconductors (Extrinsic semiconductors) holes are majority charge carriers.
2. **(c)** $I = \frac{V}{R} = \frac{20}{2 \times 10^3} = 10 \times 10^{-3} A = 10$ mA
3. **(d)** Donor level close to energy band is in case of *n*-type semi-conductor.
4. **(a)** Aluminium is trivalent impurity
5. **(a)**
6. **(c)** The given circuit is full wave rectifier.
7. **(c)** 8. **(c)**
9. **(b)** Current flow is possibe and $i = \frac{V}{R} = \frac{(4-1)}{300} = 10^{-2}$ A
10. **(a)** At room temperature, few bonds breaks and electron hole pair generates inside the semiconductor.
11. **(a)** The output ac voltage is 2.0 V. So, the ac collector current $i_C = 2.0/2000 = 1.0$ mA.
The signal current through the base is, therefore given by $i_B = i_C/\beta = 1.0$ mA$/100 = 0.010$ mA.

The dc base current has to be 10 × 0.010 = 0.10 mA.
$R_B = (V_{BB} - V_{BE})/I_B$.
Assuming $V_{BE} = 0.6$ V, $R_B = (2.0 . 0.6)/0.10 = 14\ k\Omega$.

12. **(b)** The dc collector current $I_C = 100 \times 0.10 = 10$ mA.

13. **(a)** $F = (W + X).(W + Y) = W.(X + Y)$

14. **(d)** Voltage regulator needed constant voltage and so *de* part is most relevant for its operation.

15. **(d)** Here $y = \overline{(\overline{A} + \overline{B})} = \overline{\overline{A}}.\overline{\overline{B}} = A \cdot B$. Thus it is an AND gate for which truth table is

A	B	y
0	0	0
0	1	0
1	0	0
1	1	1

16. **(b)** In case (1) first PN junction is forward bias while second one is in reverse bias.

17. **(a)** Current I = 4.8 mA = 4.8×10^{-3} A
Width b = 4×10^{-3} m, Thickness t = 25×10^{-5} m
Length $\ell = 6 \times 10^{-2}$ m
Free electron density n = $10^{22}/m^3$.
The current density J = I/A
Area = b × t = $4 \times 10^{-3} \times 25 \times 10^{-5} = 10^{-6}\ m^2$

So, current density $J = \frac{I}{A} = \frac{4.8 \times 10^{-3}}{10^{-6}} = 4.8 \times 10^3\ A/m^2$.
Suppose the drift velocity is V_d then $I = neAV_d$.

$$V_d = \frac{4.8 \times 10^{-3}}{10^{22} \times 1.6 \times 10^{-19} \times 10^{-6}} = 3\ m/sec$$

Now the time taken by the electron to travel full length of the sample $t = \frac{\text{distance}}{\text{speed}} = \frac{\ell}{V_d} = \frac{6 \times 10^{-2}}{3} = 2 \times 10^{-2}$ sec

18. **(b)** We know that a single *p-n* junction diode connected to an *a-c* source acts as a half wave rectifier [Forward biased in one half cycle and reverse biased in the other half cycle].

19. **(b)** The probability that a state with energy E is occupied is given by $P(E) = \frac{1}{e^{(E-E_F)/K_T} + 1}$, where E_F is the Fermi energy, T is the temperature on the Kelvin scale, and K is the Boltzmann constant. If energies are measured from the top of the valence band, then the energy associated with a state at the bottom of the conduction band is E = 1.11 eV. Furthermore, KT = (8.62×10^{-5} eV/K) (300K) = 0.02586 eV. For pure silicon, E_F = 0.555 eV and $(E - E_F)/kT$ = (0.555eV) / (0.02586eV) = 21.46. Thus,

$$P(E) = \frac{1}{e^{21.46} + 1} = 4.79 \times 10^{-10}$$

For the doped semi-conductor,
$(E - E_F)/kT$ = (0.11 eV) / (0.02586 eV) = 4.254

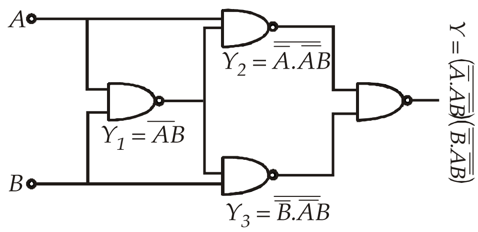
and $P(E) = \frac{1}{e^{4.254} + 1} = 1.40 \times 10^{-2}$.

20. **(a)** The energy of the donor state, relative to the top of the valence bond, is 1.11 eV – 0.15 eV = 0.96 eV. The Fermi energy is 1.11 eV – 0.11 eV = 1.00 eV. Hence,

$$(E - E_F)/kT = (0.96eV - 1.00eV)\ /(0.02586eV) = -1.547$$

and $P(E) = \frac{1}{e^{-1.547} + 1} = 0.824$

21. **(a)**

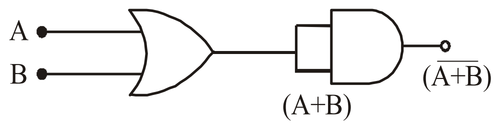


By expanding this Boolean expression

$$Y = A.\overline{B} + B.\overline{A}$$

Thus the truth table for this expression should be (1).

22. **(b)** $\overline{(A + B)}$ = NOR gate
When both inputs of NAND gate are connected, it behaves as NOT gate
OR + NOT = NOR.



23. **(a)** The final boolean expression is,

$$X = \overline{(\overline{A}.\overline{B})} = \overline{\overline{A}} + \overline{\overline{B}} = A + B \Rightarrow \text{OR gate}$$

24. **(b)**

25. **(b)** In forward biasing, the diode conducts. For ideal junction diode, the forward resistance is zero; therefore, entire applied voltage occurs across external resistance R i.e., there occurs no potential drop, so potential across R is V in forward biased.

26. **(a)** The given truth table is of
(OR gate + NOT gate) ≡ NOR gate

27. **(c)** When the collector is positive and emitter is negative w.r.t. base, it causes the forward biasing for each junction, which causes conduction of current.

28. **(a)** The current will flow through R_L when the diode is forward biased.

29. **(b)** Output of upper AND gate = $\overline{A}B$

Output of lower AND gate = $A\overline{B}$

∴ Output of OR gate, $Y = A\overline{B} + B\overline{A}$
This is boolean expression for XOR gate.

30. **(d)** Copper is a conductor, so, its resistance decreases on decreasing temperature as thermal agitation decreases whereas germanium is semiconductor, therefore, on decreasing temperature resistance increases.

31. **(c)** Study of junction diode characteristics shows that the junction diode offers a low resistance path, when forward biased and high resistance path when reverse biased. This feature of the junction diode enables it to be used as a rectifier.

32. **(b)** These gates are called digital building blocks because using these gates only (either NAND or NOR) we can compile all other gates also (like OR, AND, NOT, XOR)

33. **(b)** A NOT gate puts the input condition in the opposite order, means for high input it gives low output and for low input it gives high output. For this reason NOT gate is known as invertor circuit.