



SanDisk microSD

OEM Product Manual

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Revision History

| Date | Revision | Description |
|------------|----------|---|
| July 2008 | 1.0 | First Revision |
| March 2010 | 2.0 | Added 32GB; Removed 512MB Replaced SD2.0 with SD3.0 ACMD41 to ready after power-up updated Automatic Sleep Mode description updated Partial blocks for read not allowed for microSDHC |

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1 INTRODUCTION

1.1 General Description

The SanDisk microSD and microSDHC (SD High Capacity) Cards are flash based removable non-volatile memory devices specifically designed to meet the security, capacity, performance and environmental requirements inherent in next generation mobile phones and consumer electronic devices. The SanDisk microSD Card is based on the SD Card specification.¹ microSDHC cards (above 2GB) have both the SDHC and the Speed Class logo (Class 2, Class 4, Class 6 or Class 10) as defined by SD Specification Version 3.0.

The SanDisk microSD Card includes a faster content protection system that complies with the security of the Secure Digital Music Initiative (SDMI) standard and has a higher memory capacity. In the SanDisk microSD Card, card content is protected from illegal use by mutual authentication and a cipher algorithm. Unsecured access to the user's own content is also available.

microSD Cards are based on a 8-pin interface designed to operate in a maximum operating frequency of 50 MHz. The interface for microSD Card products allows for easy integration into any design, regardless of which type of microprocessor is used. In addition to the interface, microSD Card products offer an alternate communication-protocol based on the SPI standard.

SanDisk microSD Card Product Family provides up to 32 gigabytes (GB) of memory using flash memory chips, which were designed especially for use in mass storage applications. In addition to the mass storage-specific flash memory chip, cards in the microSD Card Product Family includes an on-board intelligent controller which manages interface protocols; security algorithms for content protection; data storage and retrieval, as well as Error Correction Code (ECC) algorithms; defect handling; power management; wear leveling and clock control.

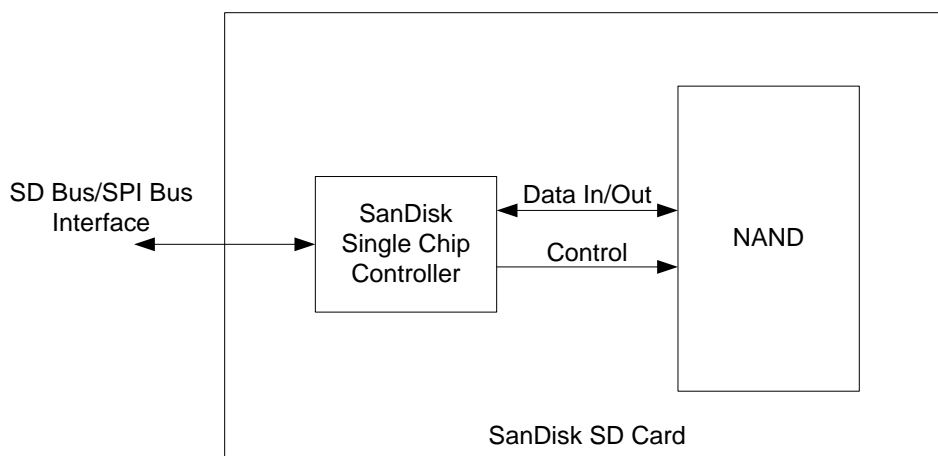


Figure 1: SD Card Block Diagram

¹ Matsushita Electric Industrial Co. Ltd., SanDisk Corporation and Toshiba Corporation (SD-3C, LLC) originally defined specifications for the SD Card. SD card specifications are now maintained, controlled and assigned by the SD-3C, LLC.

1.2 Features

General features of cards in the SanDisk microSD Card Product Family include:

- Up to 32 GB² of data storage
- SD - protocol compatible
- Supports SPI Mode
- Targeted for portable and stationary applications for secured (content protected) and unsecured data storage
- Voltage range of 2.7 to 3.6V
- Variable clock rate 0-25 MHz (standard), 0-50 MHz (high performance)
- Up to 25 MB/sec data transfer rate (using four parallel data lines)
- Memory field error correction
- Content protection mechanism that complies with highest security of SDMI standard
- Password protection
- Built-in write protection features (permanent and temporary)
- Supports card detection (insertion and removal)
- Application-specific commands

1.3 Scope

This document describes key features and specifications of the SanDisk microSD Cards as well as the information required to interface these products to a host system. Chapter 2 describes the physical and mechanical properties of cards in the SanDisk microSD Card Product Family, Chapter 3 contains the pins and register overview, and Chapter 4 gives a general overview of the SD protocol. Information about SPI Protocol can be referenced in Section 7 of the SDA Physical Layer Specification, Version 3.00.

1.4 SD Card Standard

SanDisk microSD cards are fully compatible with the SDA Physical Layer Specification, Version 3.00. This specification is available from the SD Card Association (SDA).

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² 1 megabyte (MB) = 1 million bytes; 1 gigabyte (GB) = 1 billion bytes. Some of the listed capacity is used for formatting and other functions, and thus is not available for data storage.

1.5 Functional Description

The family of SanDisk microSD cards contains a high-level, intelligent subsystem as shown in Figure 1. This intelligent (microprocessor) subsystem provides many capabilities not found in other types of memory cards. These capabilities include:

- Host independence from details of erasing and programming flash memory
- Sophisticated system for managing defects (analogous to systems found in magnetic disk drives)
- Sophisticated system for error recovery including a powerful ECC
- Power management for low power operation

1.5.1 Technology Independence

The 512-byte sector size of a card in the SanDisk microSD Card Product Family is the same as that in an IDE magnetic disk drive. To write or read a sector (or multiple sectors), the host software simply issues a read or write command to the card. The command contains the address and number of sectors to write or read. The host software then waits for the command to complete.

The host software does not get involved in the details of how the flash memory is erased, programmed or read. This is extremely important because flash devices are expected to get increasingly complex in the future. Because cards in the SanDisk microSD Card Product Family use an intelligent on-board controller, host system software will not need to be updated as new flash memory evolves. In other words, systems that support the microSD Card Product Family today will be able to access future SanDisk cards built with new flash technology without having to update or change host software.

1.5.2 Defect and Error Management

The SanDisk microSD Card Product Family contains a sophisticated defect and error management system. This system is analogous to the systems found in magnetic disk drives and in many cases offers enhancements. If necessary, SanDisk microSD Card Product Family will rewrite data from a defective sector to a good sector. This is completely transparent to the host and does not consume any user data space. The SanDisk microSD Card Product Family soft error rate specification is much better than the magnetic disk drive specification. In the extremely rare case that a read error does occur, SanDisk microSD Card Product Family has innovative algorithms to recover the data. These defect and error management systems, coupled with the solid state construction, give SanDisk microSD Card Product Family unparalleled reliability.

1.5.3 Content Protection

A detailed description of the content protection mechanism and related security SD commands can be found in the SD Security Specification from the SDA. All SD security-related commands in the SanDisk microSD Card Product Family operate in the data transfer mode.

1.5.4 Wear Leveling

Wear leveling is an intrinsic part of the erase pooling functionality of cards in the SanDisk microSD Card Product Family using NAND memory.

1.5.5 Automatic Sleep Mode

A unique feature of cards in the SanDisk microSD Card Product Family is automatic entrance and exit from sleep mode. Upon completion of user operations and subsequently needed flash management, cards enter sleep mode to conserve power. The host does not have to take any action for this to occur. However, in order to achieve the lowest sleep current, the host needs to shut down its clock to the card. In most systems, cards are in sleep mode except when accessed by the host, thus conserving power.

When the host is ready to access a card in sleep mode, any command issued to it will cause it to exit sleep, and respond.

1.5.6 Hot Insertion

Support for hot insertion will be required on the host but will be supported through the connector. Connector manufacturers will provide connectors that have power pins long enough to be powered before contact is made with the other pins. This approach is similar to that used in PCMCIA devices to allow for hot insertion.

1.6 *microSD Card Products in SD Bus Mode*

The following sections provide valuable information on cards in the SanDisk microSD Card Product Family in SD Bus mode.

Cards in the SanDisk microSD Card Product Family are fully compliant with the SDA Physical Layer Specification, Version 3.00. Card Specific Data (CSD) Register structures are compliant with CSD Structure 1.0 and 2.0.

This section covers Negotiating Operating Conditions, Card Acquisition and Identification, Card Status, Memory Array Partitioning, Read/Write Operations, Data Transfer Rate, Data Protection in Flash Cards, Write Protection, Copy Bit, and CSD Register.

Additional practical card detection methods can be found in application notes pertaining to the SDA Physical Layer Specification, Version 3.00.

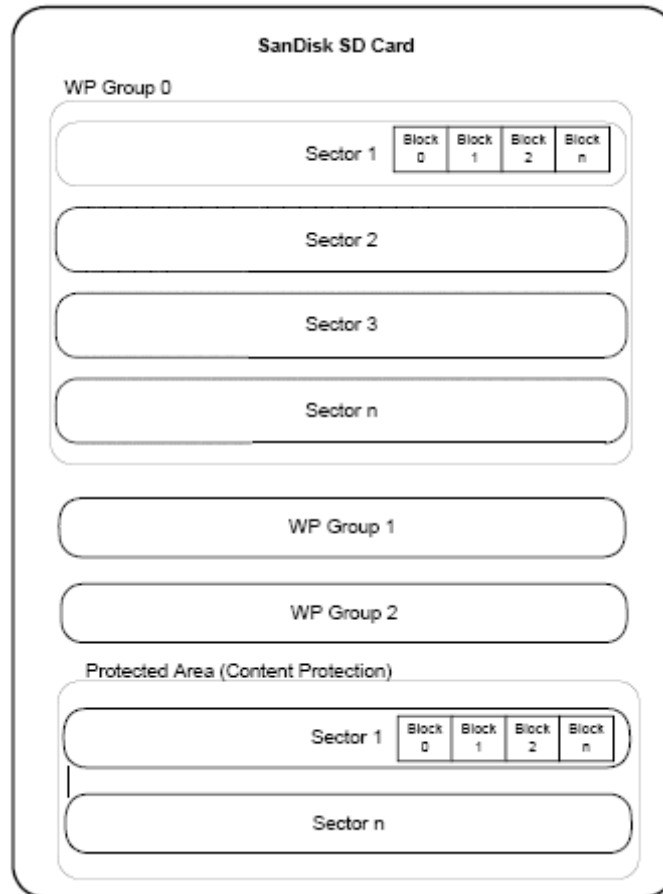


Figure 2: Memory Array Partitioning

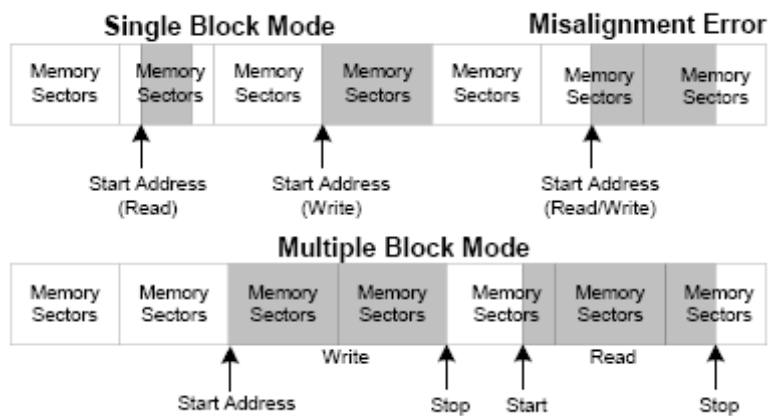


Figure 3: Data Transfer Formats

Table 1 contains descriptions for each transfer mode.

Table 1: Mode Descriptions

| Mode | Description |
|----------------|--|
| Single Block | <p>In this mode the host reads or writes one data block in a pre-specified length. The data block transmission is protected with 16-bit CRC that is generated by the sending unit and checked by the receiving unit.</p> <p>The block length for read operations is limited by the device sector size (512 bytes) but can be as small as a single byte. Misalignment is not allowed. Every data block must be contained in a single physical sector.</p> <p>The block length for write operations must be identical to the sector size and the start address aligned to a sector boundary.</p> |
| Multiple Block | <p>This mode is similar to the single block mode, except for the host can read/write multiple data blocks (all have the same length) that are stored or retrieved from contiguous memory addresses starting at the address specified in the command. The operation is terminated with a stop transmission command.</p> <p>Misalignment and block length restrictions apply to multiple blocks and are identical to the single block read/write operations.</p> |

1.7 SPI Mode

The SPI Mode is a secondary communication protocol for cards in the SanDisk microSD Card Product Family. This mode is a subset of the SD Protocol, designed to communicate with an SPI channel, commonly found in Motorola and other vendors' microcontrollers. Detailed information about SPI Mode can be found in Section 7 or the SDA Physical Layer Specification, Version 3.00.

2 PRODUCT SPECIFICATIONS

2.1 microSD Card Product Family

This section provides product specifications for the SanDisk microSD Card Product Family.

2.1.1 Typical Card Power Requirements

The values stated in Table 2 represent the SanDisk microSD Card power requirements.

Table 2: SanDisk microSD Card Power Requirements

| Mode | Maximum Value |
|--------------------------------|---------------|
| Standard Mode (25 MHz) | |
| Sleep | 350 μ A |
| Read | 100 mA |
| Write | 100 mA |
| High Performance Mode (50 MHz) | |
| Sleep | 350 μ A |
| Read | 200 mA |
| Write | 200 mA |

Note: Current consumption is measured by averaging over one (1) second. Refer to Section 6.6.3 of the SDA Physical Layer Specification, Version 3.00 for more information

2.1.2 System Performance

This section provides the system performance specifications for the SanDisk microSD Card Product Family. All performance values in Table 3 were measured under the following conditions:

- Voltage range 2.7 to 3.6V
- Temperature -25°C to 85°C
- Independent of card clock frequency

Table 3: System Performance

| Timing | Maximum Value |
|--------------------------------|---------------|
| Block Read Access Time | 100 ms |
| Block Write Access Time | 250 ms |
| ACMD41 to ready after power-up | 1 s |

2.1.3 Physical Specifications

Figure 4 and Figure 5 provide the physical dimensions of the SanDisk microSD Card. For detail dimensions and tolerances refer to SDA microSD Card Addendum, Section 3.0 Mechanical Specification for microSD Memory Card.

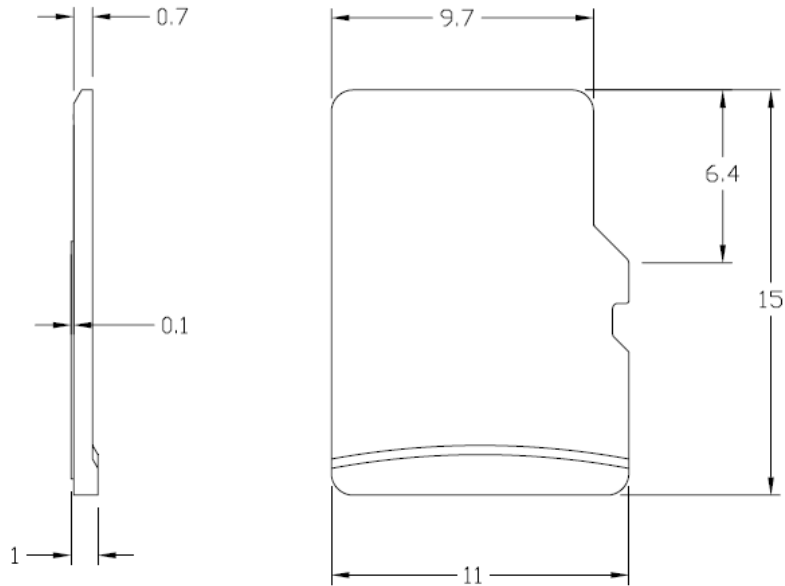


Figure 4: microSD Card Top View and Side View

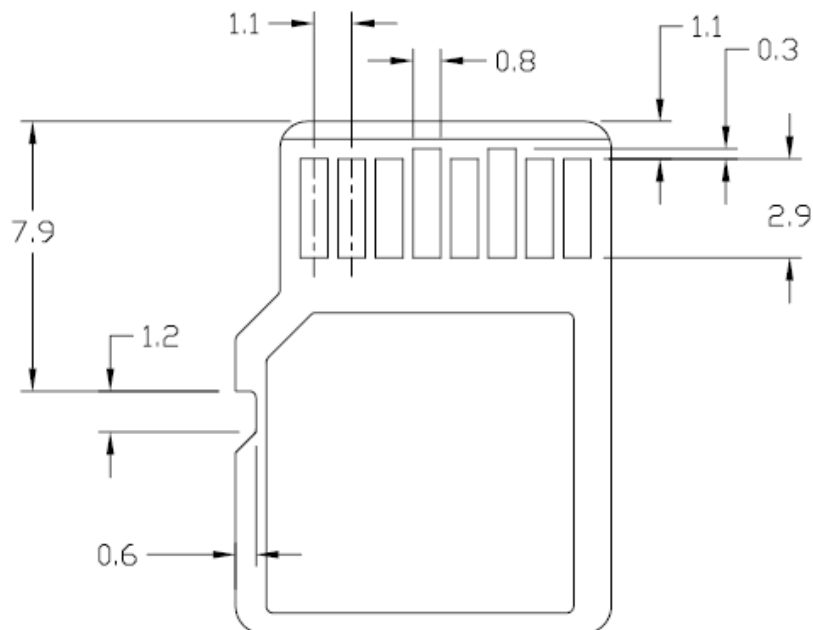


Figure 5: microSD Card Bottom View

3 INTERFACE DESCRIPTION

3.1 Pins and Registers

The SanDisk microSD Card Product Family has exposed contacts on one side. The host uses a dedicated connector to connect to microSD cards.

In Table 4, pin assignments for the SanDisk microSD Card are for SD Bus Mode. Table 5 contains pin assignments for SPI Mode.

Note: Pin assignments are provided by the SDA Physical Layer Specification, Version 3.00 and associated addendums (microSD). For more details, refer to Section 3.7 of the SDA Physical Layer Specification, Version 3.00

Table 4: SD Bus Mode Pin Assignment

| Pin No. | Name | Type | Description |
|---------|-----------------|--------|-------------------------------|
| 1 | DAT2 | I/O/PP | Data Line [bit 2] |
| 2 | CD/DAT3 | I/O/PP | Card Detect/Data Line [bit 3] |
| 3 | CMD | PP | Command/Response |
| 4 | V _{DD} | S | Supply Voltage |
| 5 | CLK | I | Clock |
| 6 | V _{SS} | S | Supply voltage ground |
| 7 | DAT0 | I/O/PP | Data Line [bit 1] |
| 8 | DAT1 | I/O/PP | Data Line [bit 2] |

- Notes:
1. Type Key: S=power supply; I=input; O=output using push-pull drivers; PP=I/O using push-pull drivers.
 2. The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after the SET_BUS_WIDTH command. It is the responsibility of the host designer to connect external pull-up resistors to all data lines even if only DAT0 is to be used. If not, there may be unexpected high current consumption due to the floating inputs of DAT1 & DAT2 (if they are not used).
 3. At power up this line has a 50KOhm pull-up enabled in the card. This resistor serves two functions: Card Detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode, it should drive the line low. For Card Detection, the host detects that the line is pulled high. The user should disconnect this pull-up with SET_CLR_CARD_DETECT (ACMD42) command during regular data transfer.

The SanDisk microSD Card pin assignments in Table 5 below are for SPI Mode

Table 5: SPI Bus Mode Pin Assignment

| Pin No. | Name | Type | Description |
|---------|-----------------|------|--------------------------|
| 1 | RSV | - | Reserved |
| 2 | CS | I | Chip select (active low) |
| 3 | DataIn | I | Data In |
| 4 | V _{DD} | S | Supply Voltage |
| 5 | SCLK | I | Clock |
| 6 | V _{SS} | S | Supply voltage ground |
| 7 | DataOUT | O/PP | Data Out |
| 8 | RSV | - | Reserved |

Each card has a set of information registers. Register descriptions and SDA references are provided in Section 5.0 of the SDA Physical Layer Specification, Version 3.00.

Table 6: microSD Card Product Family Register Overview

| Register Abbreviation | Width (in bits) | Register Name |
|-----------------------|-----------------|------------------------------|
| CID | 128 | Card identification number |
| RCA | 16 | Relative card address |
| CSD | 128 | Card specific data |
| SCR | 64 | SD configuration register |
| OCR | 32 | Operation condition register |
| SSR | 512 | SD status register |
| CSR | 32 | Card status register |

3.2 Bus Topology

The family of SanDisk microSD products supports two communication protocols: SD and SPI. For more details, refer to Section 3.5 of the SDA Physical Layer Specification, Version 3.00. Section 6 of the specification contains a bus circuitry diagram for reference.

3.2.1 SD Bus

For more details, refer to Section 3.5.1 of the SDA Physical Layer Specification, Version 3.00.

3.2.2 SPI Bus

For more details, refer to Section 3.5.2 of the SDA Physical Layer Specification, Version 3.00.

3.3 Hot Insertion and Power Protection

Refer to Section 6.1, 6.2, and 6.3 of the SDA Physical Layer Specification, Version 3.00.

3.4 Electrical Interface

The power scheme of SanDisk microSD products is handled locally in each card and in the bus master. Refer to Section 6.4 of the SDA Physical Layer Specification, Version 3.00.

3.4.1 Power Up

Power must be applied to the VDD pin before any I/O pin is set to logic HIGH. In other words, CMD, CLK, and DAT0-3 must be at zero (0) volts when power is applied to the VDD pin. For more information, refer to Section 6.4.1 of the SDA Physical Layer Specification, Version 3.00.

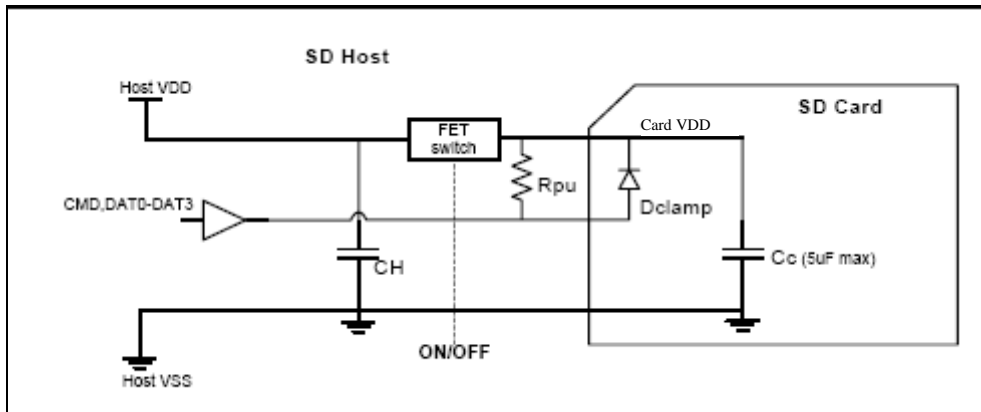


Figure 6: Recommended Power Control Scheme

The recommended power control scheme for SanDisk microSD cards is illustrated in Figure 6. Most card connectors have a card detect switch that signals the SD host when the card is inserted. After the host is aware of the card insertion, it turns on the FET switch to apply power to card's VDD pin.

Once the card is inserted and all card pins are making contact, there should be a delay before the FET switch is turned on.

Note: Because there are clamping diodes on the CMD, CLK, and DAT0-3 pins, it is crucial to ensure that CLK, CMD, and DAT0-3 are at zero (0) volts during the delay and before the FET switch is turned on. If any I/O pin, (CMD, CLK, or DAT0-3) goes above zero volts during the delay and before power reaches the card VDD pin, it will forward bias the clamping diodes and can cause the card to go into an unknown state.

It is the host's responsibility to make sure power gets to VDD before CMD, CLK, or DAT0-3 go above zero volts.

3.4.2 Bus Operating Conditions

SPI Mode bus operating conditions are identical to SD Card Bus Mode operating conditions. For details, see Section 6.6 of the SDA Physical Layer Specification, Version 3.00.

3.4.3 Bus Timing (Standard Mode)

See Section 6.6.6 of the SDA Physical Layer Specification, Version 3.00.

3.4.4 Bus Timing (High Performance Mode)

See Section 6.6.7 of the SDA Physical Layer Specification, Version 3.00.

3.5 microSD Card Product Family Registers

There is a set of eight registers within the card interface. However, the DSR Register is optional and is not used in the SanDisk microSD Card Product Family. For specific information about all registers, refer to Section 5 of the SDA Physical Layer Specification, Version 3.00.

3.5.1 Operation Conditions Register

The Operation Conditions Register (OCR) stores a card's VDD voltage profile. Refer to Section 5.1 of the SDA Physical Layer Specification, Version 3.00 for more information.

3.5.2 Card Identification Register

The Card Identification (CID) Register is 16 bytes long and contains the unique card identification number. It is programmed during card manufacturing and cannot be changed by card hosts. See Table 7.

Table 7: CID Register Definitions

| Name | Type | Width | CID Value | Comments |
|------------------------------|--------|-------|---|--|
| Manufacturer ID (MID) | Binary | 8 | 0x03 | Manufacturer IDs are controlled and assigned by the SD-3C, LLC |
| OEM/Application ID (OID) | ASCII | 16 | SD ASCII Code 0x53, 0x44 | Identifies the card OEM and/or the card contents. The OID is controlled and assigned by the SD-3C, LLC |
| Product Name (PNM) | ASCII | 40 | SD32G SD16G SD08G SD06G SD04G SD02G SD01G | Five-character ASCII string |
| Product Revision (PRV) | BCD | 8 | Product Revision xx | See Section 5.2 in the SDA Physical Layer Specification, Version 3.00. |
| Serial Number (PSN) | Binary | 32 | Product serial number | 32-bit unsigned integer |
| Reserved | - | 4 | - | - |
| Manufacturer Date Code (MDT) | BCD | 12 | Manufacture date (for example, April 2001=0x014) | Manufacturing date–yym (offset from 2000) |
| CRC7 Checksum (CRC) | Binary | 7 | CRC7 | Calculated |
| Not used, always 1 | - | 1 | - | - |

3.5.3 Card Specific Data Register

The Card Specific Data (CSD) Register configuration information is required to access card data. The CSD defines the data format, error correction type, maximum data access time, etc. The field structures of the CSD Register vary depending on the physical specifications and card capacity. The CSD_STRUCTURE field in the CSD Register indicates which structure version is used. Table 8 shows the version number as it relates to the CSD structure. Refer to Section 5.3.1 of the SDA Physical Layer Specification, Version 3.00 for more information.

Table 8: CSD Register Structure

| CSD_Structure | CSD Structure Version | Valid for SD Card Physical Specification / Card Capacity |
|---------------|-----------------------|--|
| 0 | CSD Version 1.0 | Version 1.01 to 1.10 Version 2.00/Standard Capacity |
| 1 | CSD Version 2.0 | Version 2.00/High Capacity |
| 2-3 | Reserved | - |

Table 9 provides an overview of the CSD Register. More field-specific information can be found in Section 5.3.2 of the SDA Physical Layer Specification, Version 3.00.

Table 9: CSD Register (CSD Version 1.0)

| Field | CSD Value | Description |
|--------------------|---|---|
| CSD_STRUCTURE | 1.0 | CSD Structure |
| - | - | Reserved |
| TAAC | 1.5 msec | Data read access-time-1 |
| NSAC | 0 | Data read access-time-2 in CLK cycles (NSAC*100) |
| TRANS_SPEED | Standard Mode 25 MHz High Performance Mode 50MHz | Maximum data transfer rate |
| CCC | All (inc. WP, lock/unlock) | Card command classes |
| READ_BL_LEN | 2G = 0xA Up to 1G – 0x9 | Maximum read data block length |
| READ_BL_PARTIAL | No | Partial blocks for read not allowed for microSDHC |
| WRITE_BLK_MISALIGN | No | Write block misalignment |
| READ_BLK_MISALIGN | No | Read block misalignment |
| DSR_IMP | No | DSR implemented |
| - | - | Reserved |
| C_SIZE | Secured | Device size |
| 64 MB | 0xEDF | |
| 128 MB | 0xF03 | |
| 256 MB | 0xF13 | |
| 512 MB | 0xF1E | |
| 1 GB | 0xF22 | |
| 2 GB | 0xF24 | |
| VDD_R_CURR_MIN | 100 mA | Maximum read current @V _{DD} min |
| VDD_R_CURR_MAX | 80 mA | Maximum read current @V _{DD} max |
| VDD_W_CURR_MIN | 100 mA | Maximum write current @V _{DD} min |

| Field | CSD Value | Description |
|--------------------|--|--|
| VDD_W_CURR_MAX | 80 mA | Maximum write current @V _{DD} max |
| C_SIZE_MULT | 2G=2048 1G=1024 512=512 256=256 128=128 64=64 | Device size multiplier |
| ERASE_BLK_EN | Yes | Erase single block enable |
| SECTOR_SIZE | 31 blocks | Erase sector size |
| WP_GRP_SIZE | 127 sectors | Write protect group size |
| WP_GRP_ENABLE | Yes | Write protect group enable |
| Reserved | - | Reserved for MMC compatibility |
| R2W_FACTOR | X16 | Write speed factor |
| WRITE_BL_LEN | 0x9 | Maximum write data block length |
| WRITE_BL_PARTIAL | No | Partial blocks for write allowed |
| - | - | Reserved |
| FILE_FORMAT_GRP | 0 | File format group |
| COPY | Has been copied | Copy flag (OTP) |
| PERM_WRITE_PROTECT | Not protected | Permanent write protection |
| TMP_WRITE_PROTECT | Not protected | Temporary write protection |
| FILE_FORMAT | HD w/partition | File format |
| Reserved | - | Reserved |
| CRC | CRC7 | CRC |
| - | - | Not used, always "1" |

Refer to Sections 5.3.2 and 5.3.3, of the SDA Physical Layer Specification, Version 3.00 for more detailed information.

Table 10: CSD Register (CSD Version 2.0)

| Field | CSD Value | Description |
|--------------------|---|---|
| CSD_STRUCTURE | 2.0 | CSD Structure |
| - | - | Reserved |
| TAAC | 1.5 msec | Data read access-time |
| NSAC | 0 | Data read access-time-2 in CLK cycles (NSAC*100) |
| TRANS_SPEED | Standard Mode 25 MHz High Performance Mode 50MHz | Maximum data transfer rate |
| CCC | All (inc. WP, lock/unlock) | Card command classes |
| READ_BL_LEN | 9 | Maximum read data block length |
| READ_BL_PARTIAL | No | Partial blocks for read not allowed for microSDHC |
| WRITE_BLK_MISALIGN | No | Write block misalignment |
| READ_BLK_MISALIGN | No | Read block misalignment |

| Field | CSD Value | Description |
|--------------------|-----------------|----------------------------------|
| DSR_IMP | No | DSR implemented |
| - | 0 | Reserved |
| C_SIZE | Secured | Device size |
| 4 GB | 0x1E5C | |
| 6 GB | 0x2D8C | |
| 8 GB | 0x3CDC | |
| 12 GB | 0x5B6C | |
| 16 GB | 0x79FC | |
| 32 GB | 0xF45C | |
| - | 0 | Reserved |
| ERASE_BLK_EN | 1 | Erase single block enable |
| SECTOR_SIZE | 64 blocks | Erase sector size |
| WP_GRP_SIZE | 000000b | Write protect group size |
| WP_GRP_ENABLE | No | Write protect group enable |
| Reserved | - | Reserved for MMC compatibility |
| R2W_FACTOR | X4 | Write speed factor |
| WRITE_BL_LEN | | Maximum write data block length |
| WRITE_BL_PARTIAL | No | Partial blocks for write allowed |
| - | - | Reserved |
| FILE_FORMAT_GRP | 0 | File format group |
| COPY | Has been copied | Copy flag (OTP) |
| PERM_WRITE_PROTECT | Not protected | Permanent write protection |
| TMP_WRITE_PROTECT | Not protected | Temporary write protection |
| FILE_FORMAT | HD w/partition | File format |
| Reserved | - | Reserved |
| CRC | CRC7 | CRC |
| - | - | Not used, always "1" |

3.5.4 Card Status Register

The Card Status Register (CSR) transmits the card's status information (which may be stored in a local status register) to the host. The CSR is defined in Section 4.10.1 in the SDA Physical Layer Specification, Version 3.00.

3.5.5 SD Status Register

The SD Status Register (SSR) contains status bits that are related to the microSD Card proprietary features and may be used for future applications. The SD Status structure is described in Section 4.10.2 in the SDA Physical Layer Specification, Version 3.00.

3.5.6 Relative Card Address Register

The 16-bit Relative Card Address (RCA) Register carries the card address published by the card during the card identification. Refer to Section 5.4 in the SDA Physical Layer Specification, Version 3.00 for more information.

3.5.7 SD Card Configuration Register

The SD Card Configuration Register (SCR) is in addition to the CSD Register. The SCR provides information about special features in the SanDisk SD Card products. For more information, refer to Section 5.6 in the SDA Physical Layer Specification, Version 3.00.

3.5.8 microSD Card Product Family Registers in SPI Mode

All card registers are accessible in SPI Mode. Their format is identical to the format in the SD Bus Mode; however a few fields are irrelevant in SPI Mode. In SPI Mode, the Card Status Register also has a different, shorter format. Refer to Section 7.4 in the SDA Physical Layer Specification, Version 3.00 for more details.

3.5.9 Data Interchange Format and Card Sizes

In general, a file system provides structure for data in SanDisk microSD Card products. The SD Card File System Specification, published by the SDA, describes the file format system that is implemented in the SanDisk microSD Card products. In general, each card is divided into two separate DOS-formatted partitions as follows:

- User Area—used for secured and non-secured data storage and can be accessed by the user with regular read/write commands.
- Security Protected Area—used by content protection applications to save security related data and can be accessed by the host using the secured read/write command after doing authentication as defined in the SD Security Specification. The security protected area size is defined by SanDisk as approximately one percent of the total size of the card.

Table 11: User Area DOS Image Parameters

| Capacity | Total LBAs | No. of Partition System Area Sectors | Total Partition Sectors | User Data Sectors | User Data Bytes |
|----------|------------|--------------------------------------|-------------------------|-------------------|-----------------|
| 32GB | 62333952 | 16384 | 62,325,760 | 62,309,376 | 31,902,400,512 |
| 16 GB | 31,116,288 | 8192 | 31,108,096 | 31,099,904 | 15,923,150,848 |
| 8 GB | 15,523,840 | 8192 | 15,515,648 | 15,507,456 | 7,939,817,472 |
| 4 GB | 7,744,512 | 8192 | 7,736,320 | 7,728,128 | 3,956,801,536 |
| 2 GB | 3,862,528 | 505 | 3,858,489 | 3,857,984 | 1,975,287,808 |
| 1 GB | 1,930,240 | 505 | 1,929,177 | 1,928,672 | 987,480,064 |

4 MICROSD CARD PROTOCOL DESCRIPTION

4.1 General Description

SD Protocol information for cards in the SanDisk microSD Card Product Family is contained in this chapter; information includes SD bus protocol, card identification, and a functional description.

4.2 SD Bus Protocol

Communication over the SD bus is based on command and data-bit streams initiated by a start bit and terminated by a stop bit. See Section 3.6.1 of the SDA Physical Layer Specification, Version 3.00 for details.

4.3 Functional Description

In the SanDisk microSD Card Product Family, the host controls all communication between itself and the cards. To demonstrate how this communication works, this section provides a general overview of the card identification and data transfer modes; commands; card dependencies; various card operation modes and restrictions for controlling the clock signal. All SD Card commands, together with corresponding responses, state transitions, error conditions, and timings are also provided. For detailed information, refer to Section 4 of the SDA Physical Layer Specification, Version 3.00.

4.3.1 Card Identification Mode

In Card Identification Mode, the host resets all cards, validates operation voltage range, identifies and requests cards to publish a relative card address. For more information see Section 4.2 in the SDA Physical Layer Specification, Version 3.00.

4.3.2 Data Transfer Mode

In Data Transfer Mode, the host may operate SanDisk microSD Card Product Family cards in the fPP frequency range. In the SDA Physical Specification, this section includes information about data read and write, erase, write-protect management, card lock/unlock operations, application-specific commands, switch function command, high-speed mode, command system, and the Send Interface Condition command (CMD8). CMD8 is part of identification mode and command functional differences in high capacity microSD cards. For more detailed information, refer to Section 4.3 of the SDA Physical Layer Specification, Version 3.00.

4.3.3 Clock Control

The host can use the bus clock signal in SanDisk microSD cards to switch them to energy saving mode or to control data flow on the bus. See Section 4.4 of the SDA Physical Layer Specification, Version 3.00.

4.3.4 Cyclic Redundancy Codes

The Cyclic Redundancy Check (CRC) protects against transmission errors that may occur on the bus in SanDisk microSD Card Product Family cards. Detailed information and examples for CRC7 and CRC16 are provided in Section 4.5 of the SDA Physical Layer Specification, Version 3.00.

4.3.5 Error Conditions

See Section 4.6 of the SDA Physical Layer Specification, Version 3.00.

4.3.6 Commands

See Section 4.7 of the SDA Physical Layer Specification, Version 3.00 for detailed information about card commands in the SanDisk microSD Card Product Family.

4.3.7 Card State Transition

In microSD cards, the state transition is dependent on the received command. The transition is defined in Section 4.8 of the SDA Physical Layer Specification, Version 3.00 along with responses sent on the command line.

4.3.8 Timing Diagrams and Values

See Section 4.12 of the SDA Physical Layer Specification, Version 3.00.

4.3.9 Speed Class Specification

SDA speed class specification classifies SDHC card minimum write performance by speed class number and offers the method to test performance. For more information, refer to Section 4.13 of the SDA Physical Layer Specification, Version 3.00.

4.3.10 Erase Timeout Calculation

See Section 4.14 of the SDA Physical Layer Specification, Version 3.00.

5 MARKING

BBB: Capacity

ZZ: GB or MB

YY: Year

DDD: Day

XXXXXL###: Internal use

MADE IN XXXXX: Country of origin i.e. 'TAIWAN' or 'CHINA'

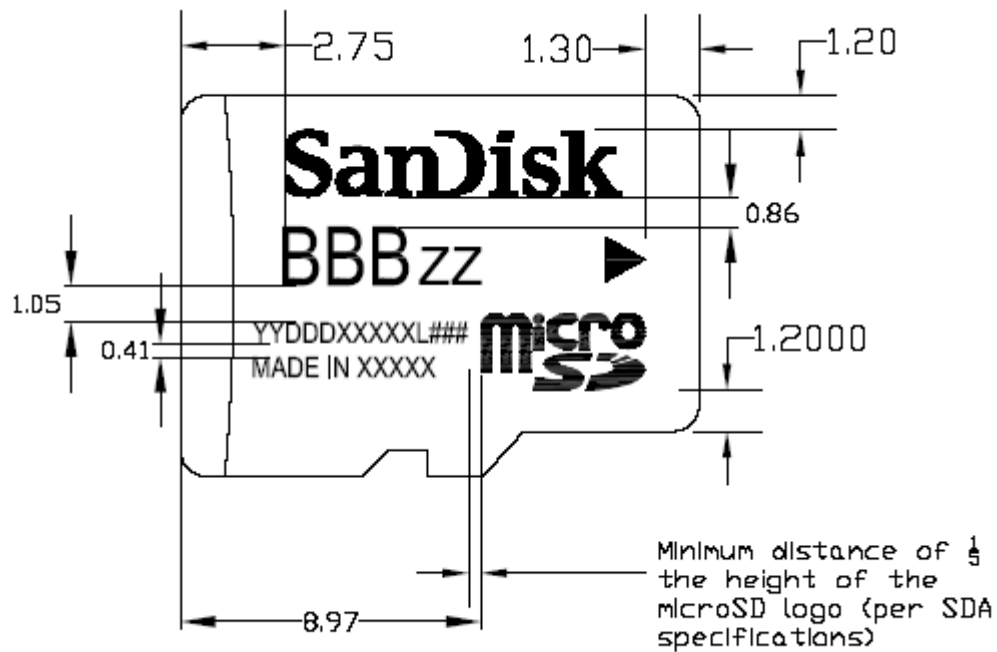


Figure 7: microSD (512MB, 1GB and 2GB) Marking

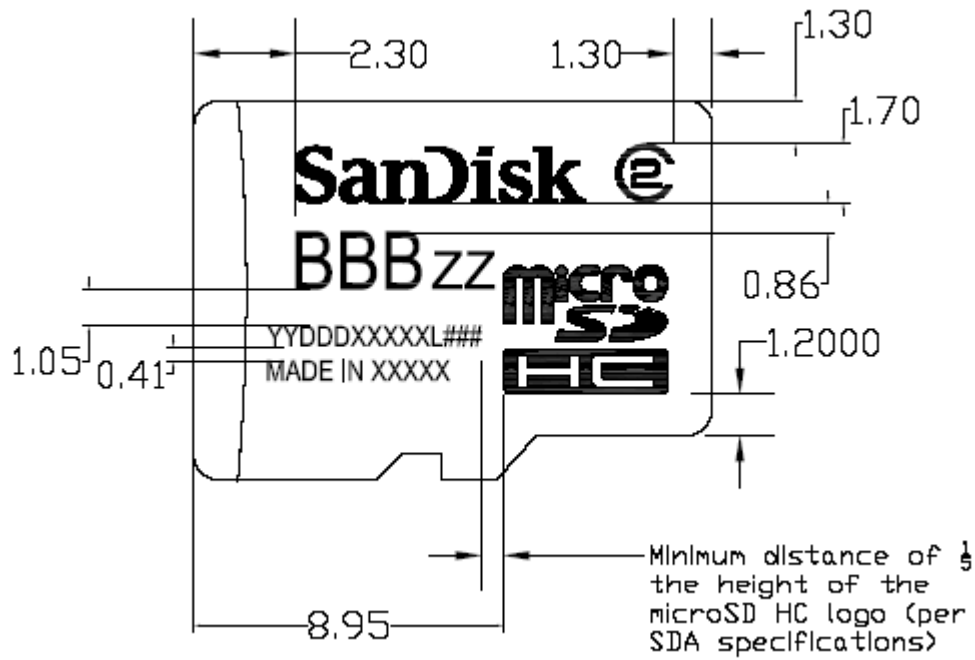


Figure 8: microSDHC (4GB, 8GB, 16GB and 32GB) Marking

6 ORDERING INFORMATION

To order SanDisk products directly from SanDisk, please contact your local sales office.

| Part Number | Capacity |
|-------------|----------|
| SDSDQ-1024 | 1 GB |
| SDSDQ-2048 | 2 GB |
| SDSDQ-4096 | 4 GB |
| SDSDQ-8192 | 8 GB |
| SDSDQ-016G | 16 GB |
| SDSDQ-032G | 32 GB |